Section 6 Typical Applications

6.1 Audio Power Amplifier Uses

6.1.1 Linear Power Amplifier

1. Design of output stage (design of power supply voltage V_{DD})

   Figure 6-1 shows an equivalent circuit of the output stage. R_{on} is a drain-to-source equivalent resistance when the power MOS FET is on, and according to the 2SK1057/2SJ161 specification it is:

$$R_{on} = \frac{V_{DS(on)}}{I_D} = \frac{12}{7} = 1.71\ \Omega$$

   The peak current I_p flowing through load R_L = 8 Ω at P_{out} = 100 W is calculated from mean current I as follows:

$$I_P = \sqrt{2} \cdot I = \sqrt{\frac{2\,P_O}{R_L}}$$

$$= \sqrt{\frac{200}{8}} = 5\ A$$

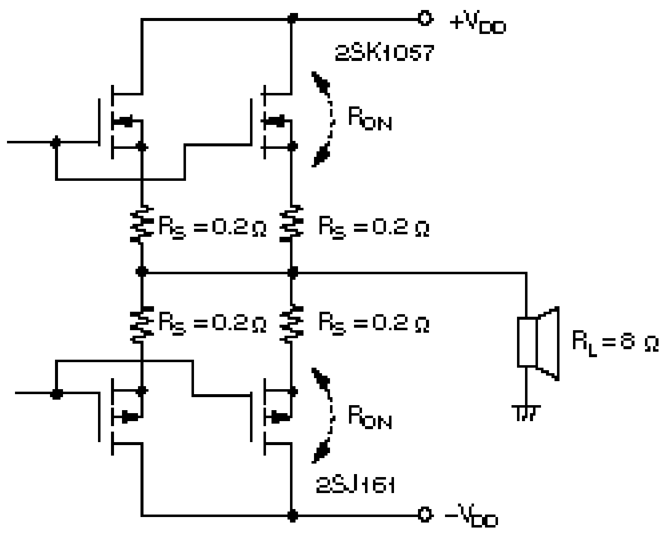

Figure 6-1 Equivalent Circuit of Power MOS FET Output Stage

Thus, if the transformer regulation is estimated at 20% and the AC line fluctuation at ±15%, then the power supply voltage V_{DD} is given as:

$$V_{DD} = 1.2 \times 1.15 \left\{R_L + \frac{(R_{on} + R_S)}{2}\right\} I_P$$
$$\approx 61.8 \text{ V}$$

In figure 6-3, the power supply of the power stage is used also by the voltage amplifier stage, so the voltage is set at ±65 V including the gate-to-source “on” voltage at P_{out} = 100 W.

In the case of the D Series 2SK413/2SJ118, the R_{on} value is very small (0.5 Ω), so the supply voltage required for the same output (100 W) is only 57.6 V. This enables the transformer and heat sink to be made smaller, reducing system cost.

2. Design of voltage amplifier stage

A power MOS FET can be driven by a low driving power. Fundamentally, only power for charging and discharging the gate-to-source capacitance is needed by the output stage, so a class B driver stage is not required. The driving power varies with input frequency. At 100 W output and 100 kHz frequency, it would be very small as follows.

$Pin = f\ Ciss\ V_{GS}^2 = 100 \times 10^3 \times 900 \times 10^{-12} \times 6^2 = 3.24$ mW

Therefore, an output-stage power MOS FET can be driven directly by a class A predriver (voltage amplifier stage) such as that used in a bipolar transistor amplifier. By eliminating the class B driver, the number of components can be reduced, and impairment of the amplifier’s performance by the driver itself can be avoided.

Moreover, the number of transfer function (open loop gain and frequency characteristics) poles decreases, and the stagger ratio can easily be increased. Consequently, the stability against oscillation is improved. Transistors for the voltage amplifier stage are required to have a high breakdown voltage, low Cob (collector output capacitance) and high f_T (gain-bandwidth product).

3. Open loop voltage gain

The transconductance $|y_{fs}|$ of power MOS FETs is as large as 1.0 to 2.5 S (typical). Yet it is only a fraction of that of bipolar transistors.

For example, the $|y_{fs}|$ of bipolar transistors at I_C (collector current) = 1.0 A is very large, as follows.

$$|y_{fs}| = \frac{1}{r_e} = \frac{I_E}{KT/q} = \frac{1\ A}{26\ mV} \approx 38\ S$$

Where

r_e: Emitter equivalent resistance
K: Boltzmann constant
T: Absolute temperature
q: Electron charge
I_E: Emitter bias current

When a power device is used in a source follower circuit (in a bipolar transistor circuit the equivalent is an emitter follower), the relationship between input and output is as follows:

$$\frac{\text{Output}}{\text{Input}} \approx \frac{R_L}{R_L = 1/|y_{fs}|}$$

(See figure 6-2.)

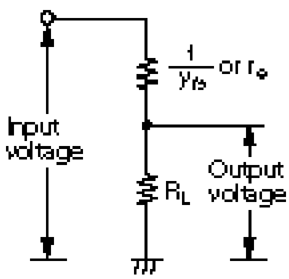

Figure 6-2 Source Follower Input and Output

Only the nonlinear component of this equation, $1/|y_{fs}|$, causes distortion, with a larger $|y_{fs}|$ resulting in lower distortion. In other words, since a power MOS FET amplifier has a distortion about 20 dB larger than a bipolar transistor amplifier, it is necessary to design for larger open loop gain and larger negative feedback than in a bipolar transistor circuit.

4. Preventing parasitic oscillation

Because power MOS FETs have excellent high-frequency characteristics, they are liable to cause oscillation even in a simple circuit.

For an analysis of stability in a source follower circuit, see section 5.10 of this Application Notes. Some precautions in system design are noted below.

- Minimize the wiring between the printed circuit board and the power MOS FETs. Direct connection is recommended.
- Provide one-point grounding for the amplifier printed circuit, power supply, and speaker terminals. Use thick wiring for the power supply line and ground line.
- An output coupling coil L has the effect of reducing distortion in the high-frequency range. It also prevents oscillation which might occur when the output is loaded by capacitance. Its value should be determined experimentally.
- The printed circuit layout should flow topographically from input to output.

POWER MOSFET TRANSISTORS
Recommended Line-up for Audio Amplifier

Output Power (W)		Input Stage			Driver Stage				Output Stage	
Parallel Push-Pull	Single Push-Pull	FET	Bipolar		FET		Bipolar		FET	
			NPN	PNP	P-Ch.	N-Ch.	NPN	PNP	P-Ch.	N-Ch.
50~60		*1			2SK213 (TO-220)	2SJ76 (TO-220)	*1	*1	2SK1056	2SJ160
60~80	100~120	*1	*1	*1	2SK214 (TO-220)	2SJ77 (TO-220)	*1	*1	2SK1057	2SJ161
	120~1500		*1	*1	2SK215 (TO-220)	2SJ78 (TO-220)	*1	*1	2SK1058	2SJ162
80~100					2SK216 (TO-220)	2SJ79 (TO-220)	*1	*1	2SK2220	2SJ351
	150~200		*1	*1					2SK2221	2SJ352

Note:
*1 on request, pls contact the help line "Talk to us"

6. Application circuits

- 100-W Output; THD ≈ 0.01%, f = 100 kHz

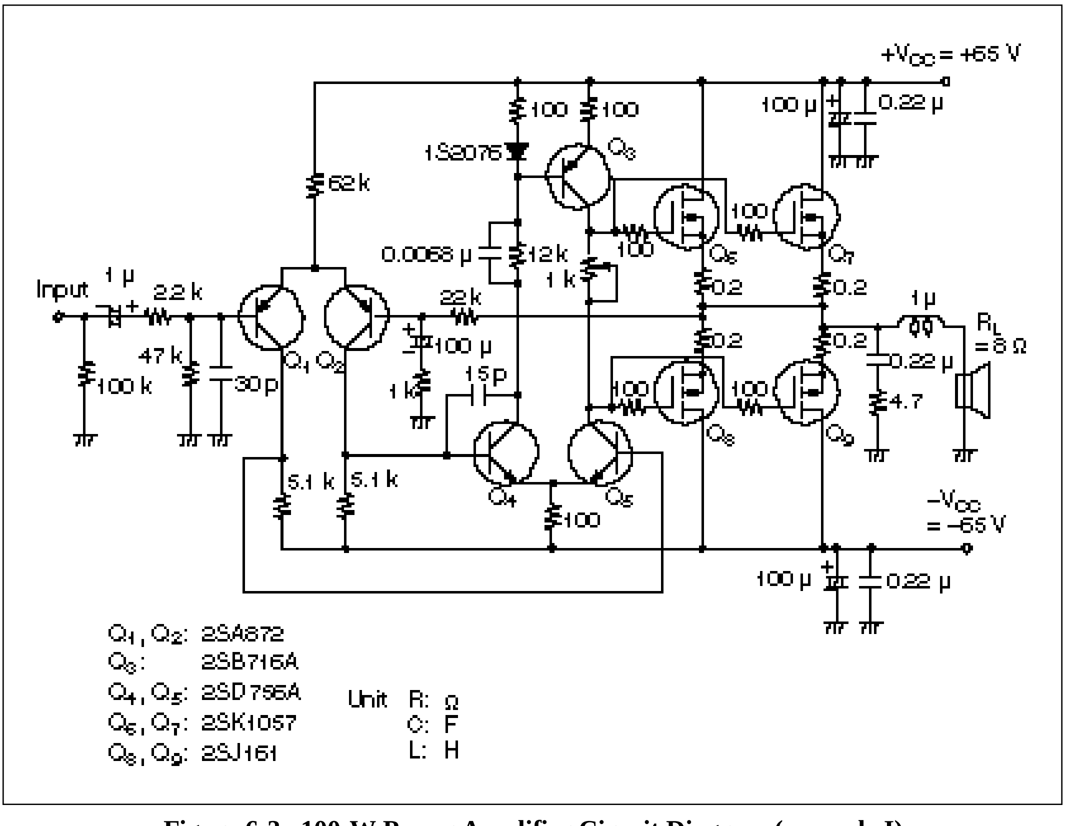

Figure 6-3 100-W Power Amplifier Circuit Diagram (example I)

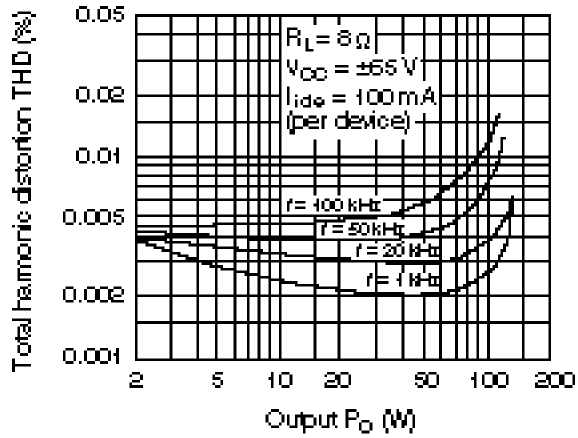

Figure 6-4 Total Harmonic Distortion vs. Output Characteristics

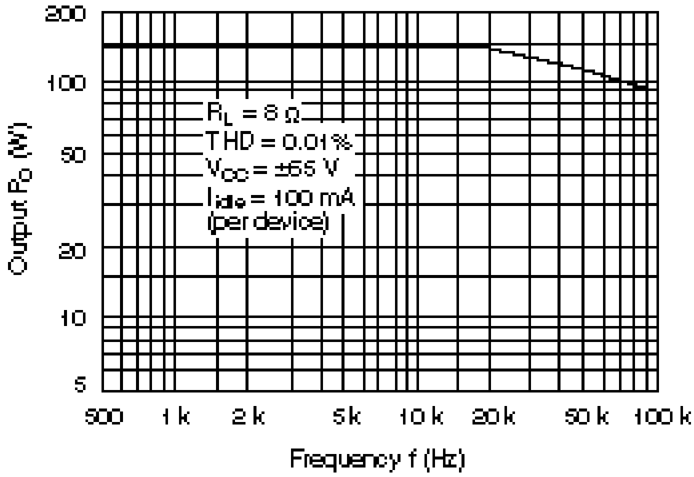

Figure 6-5 Power Band Width

- 100-W Output; THD ≈ 0.01%, f = 50 kHz

  (all-FET DC amplifier)

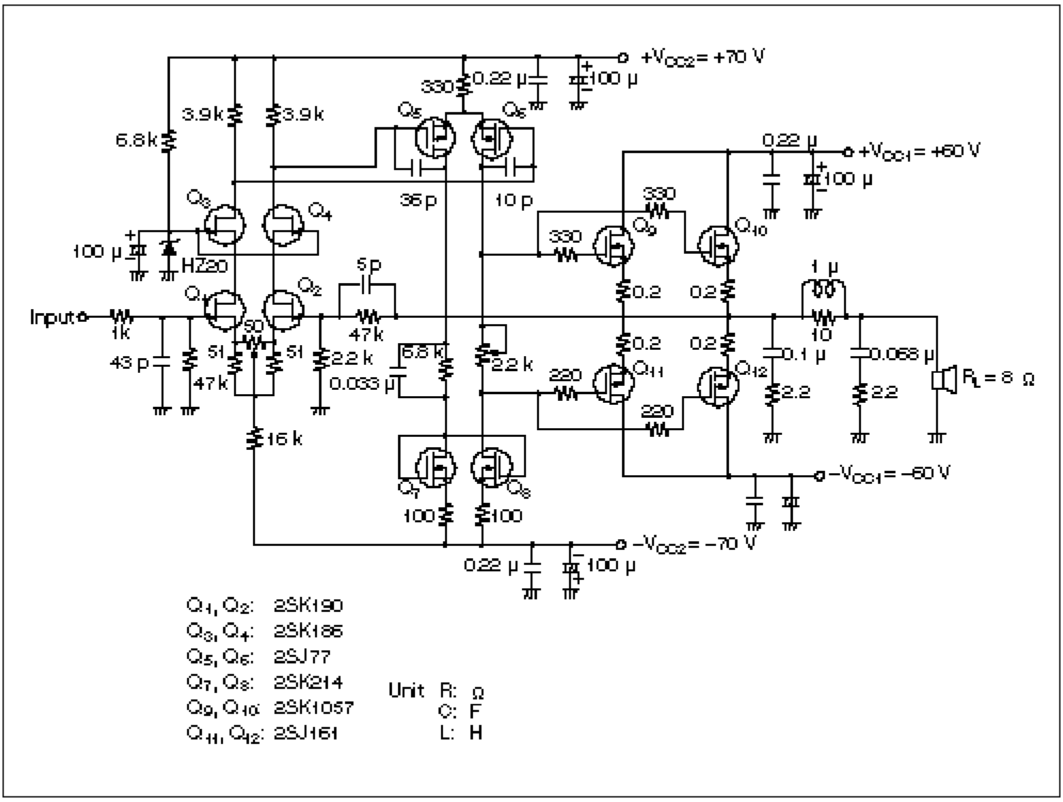

Figure 6-6 100-W All-FET Power Amplifier Circuit Diagram (example II)

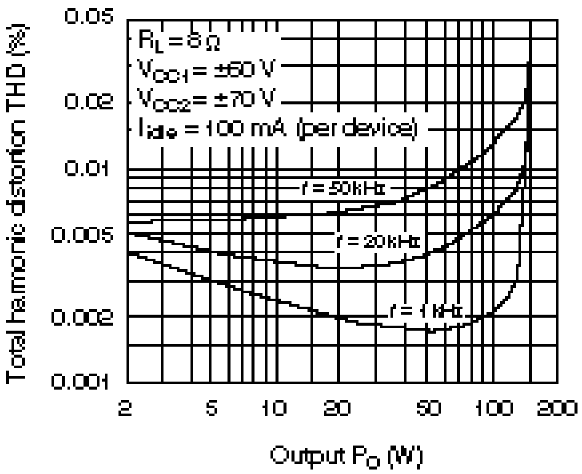

Figure 6-7 Total Harmonic Distortion vs. Output Characteristics

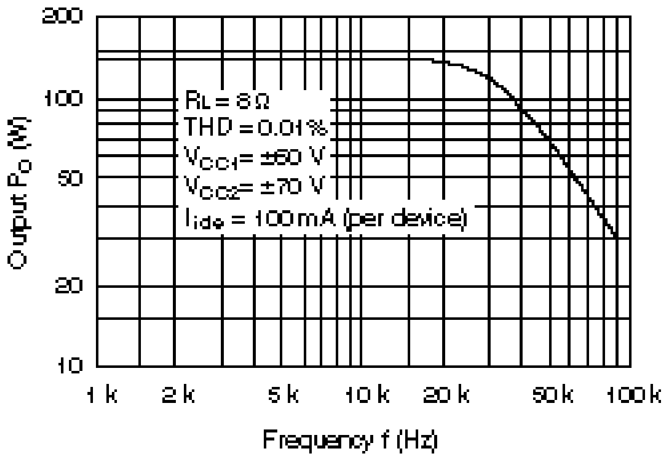

Figure 6-8 Power Band Width

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